

Replacement Sheet

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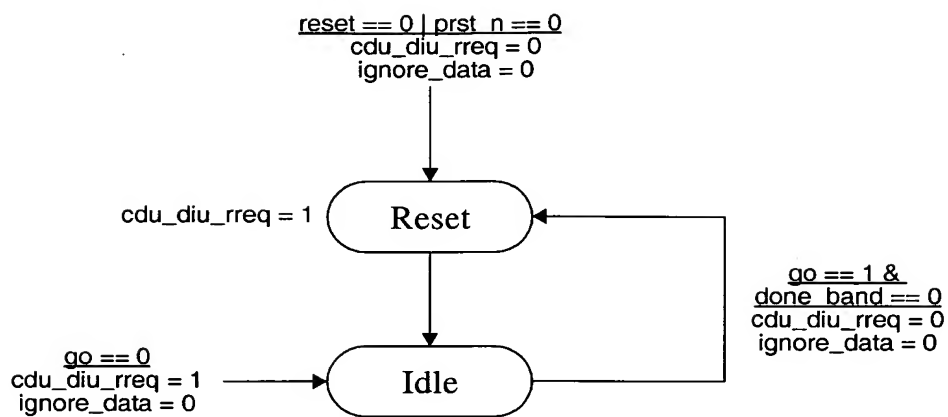


FIG. 1

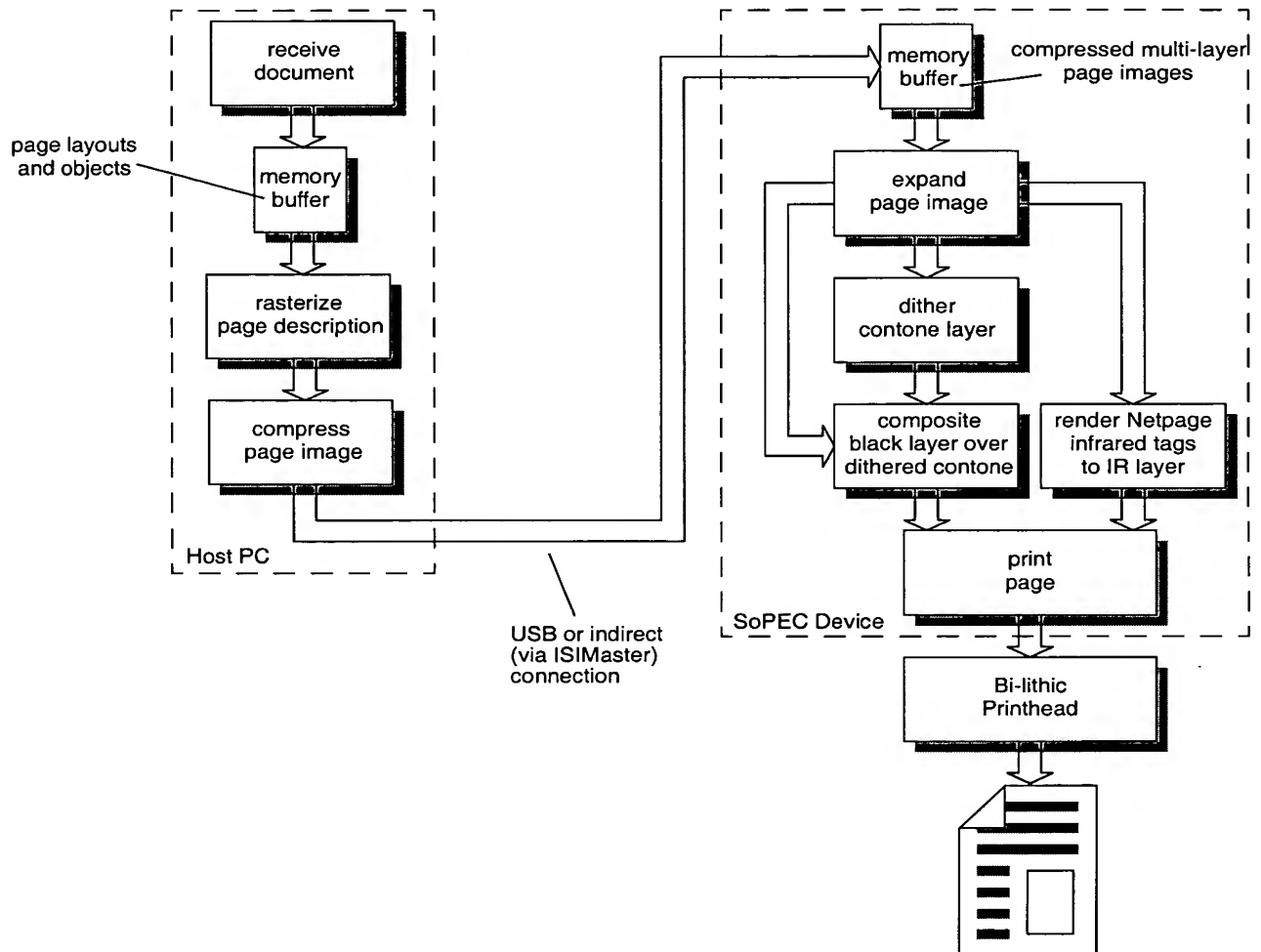


FIG. 2

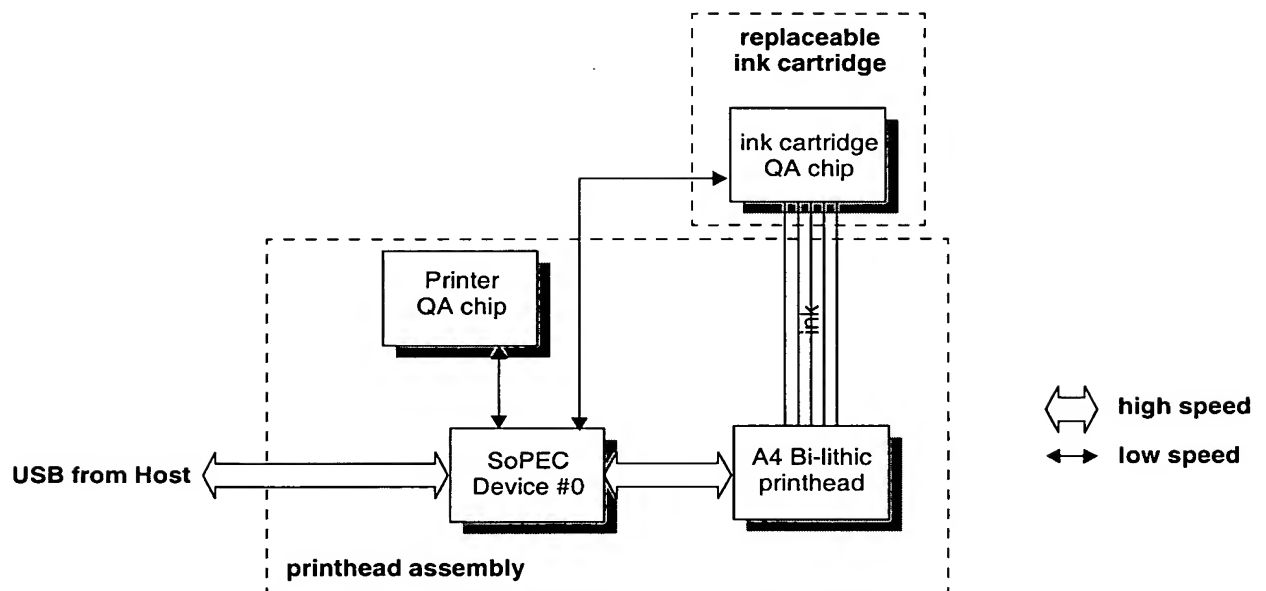


FIG. 3

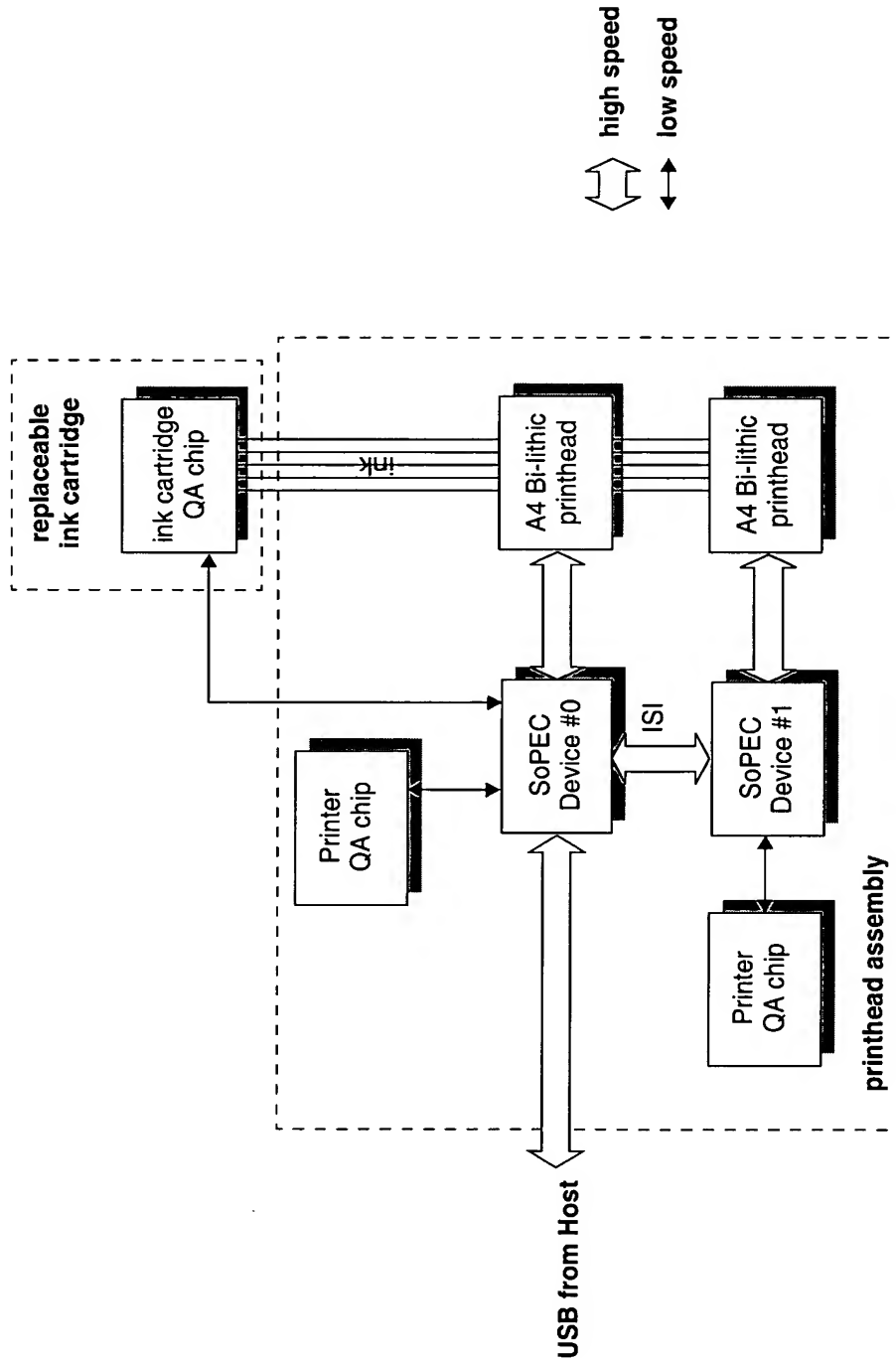


FIG. 4

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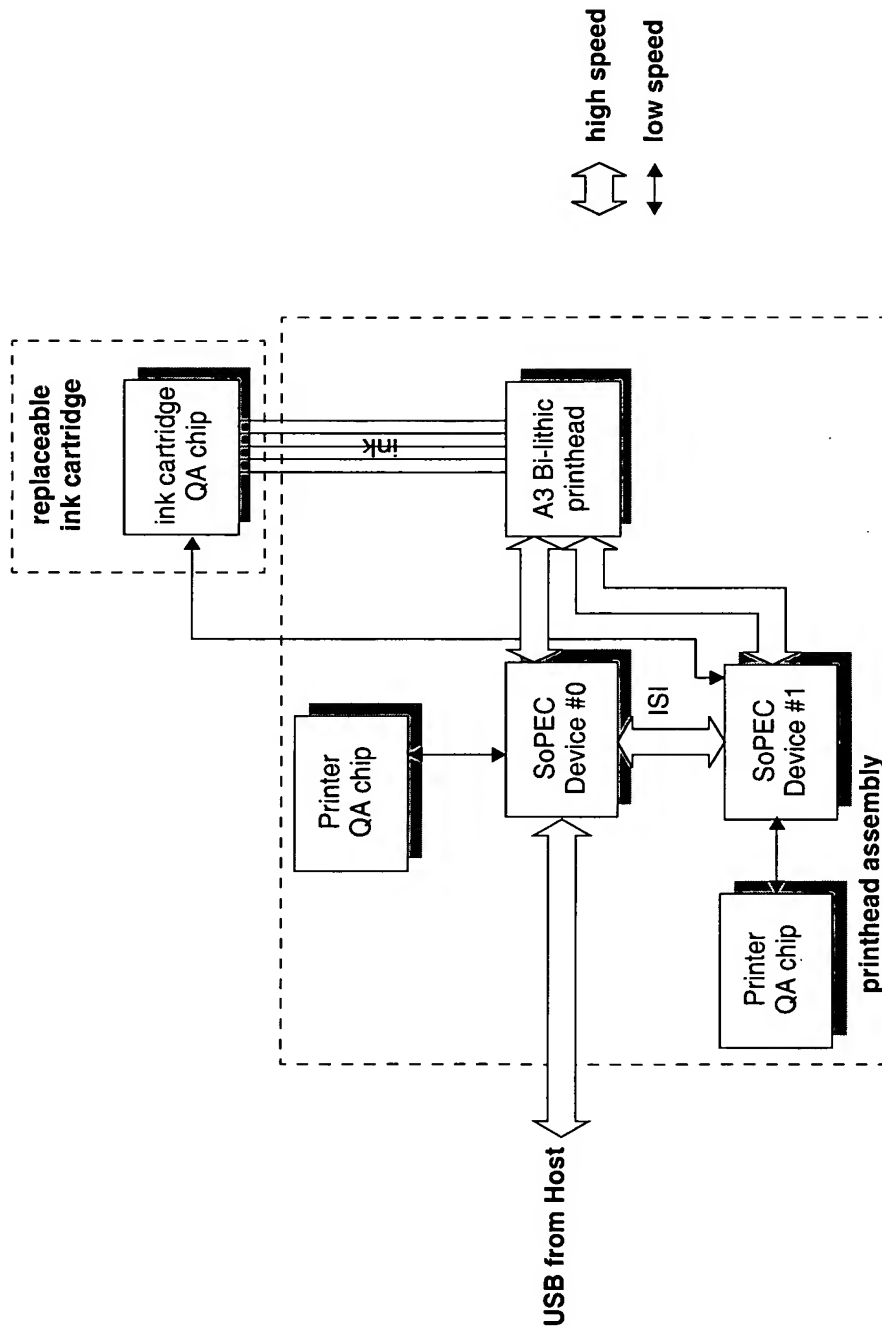


FIG. 5

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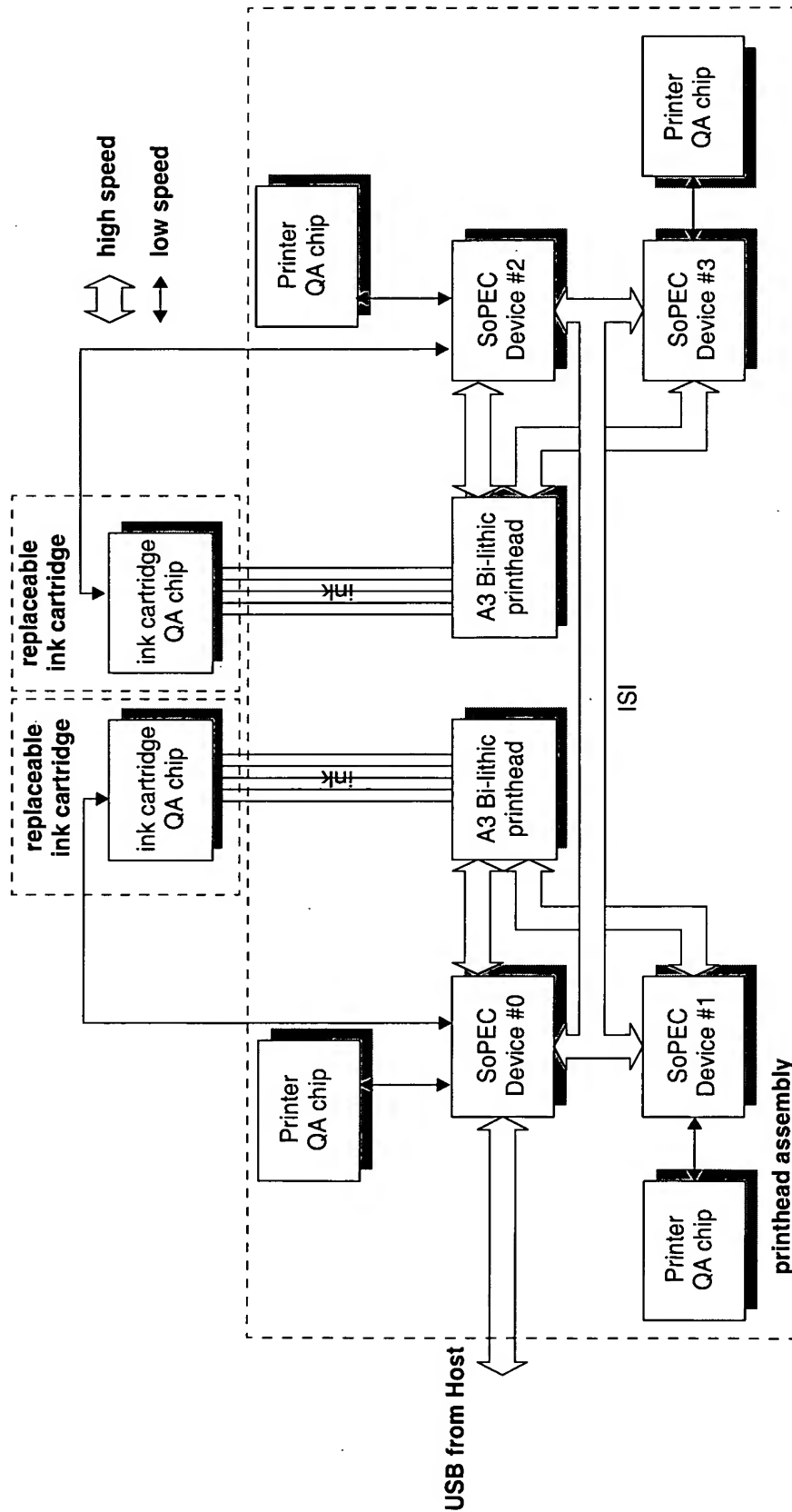


FIG. 6

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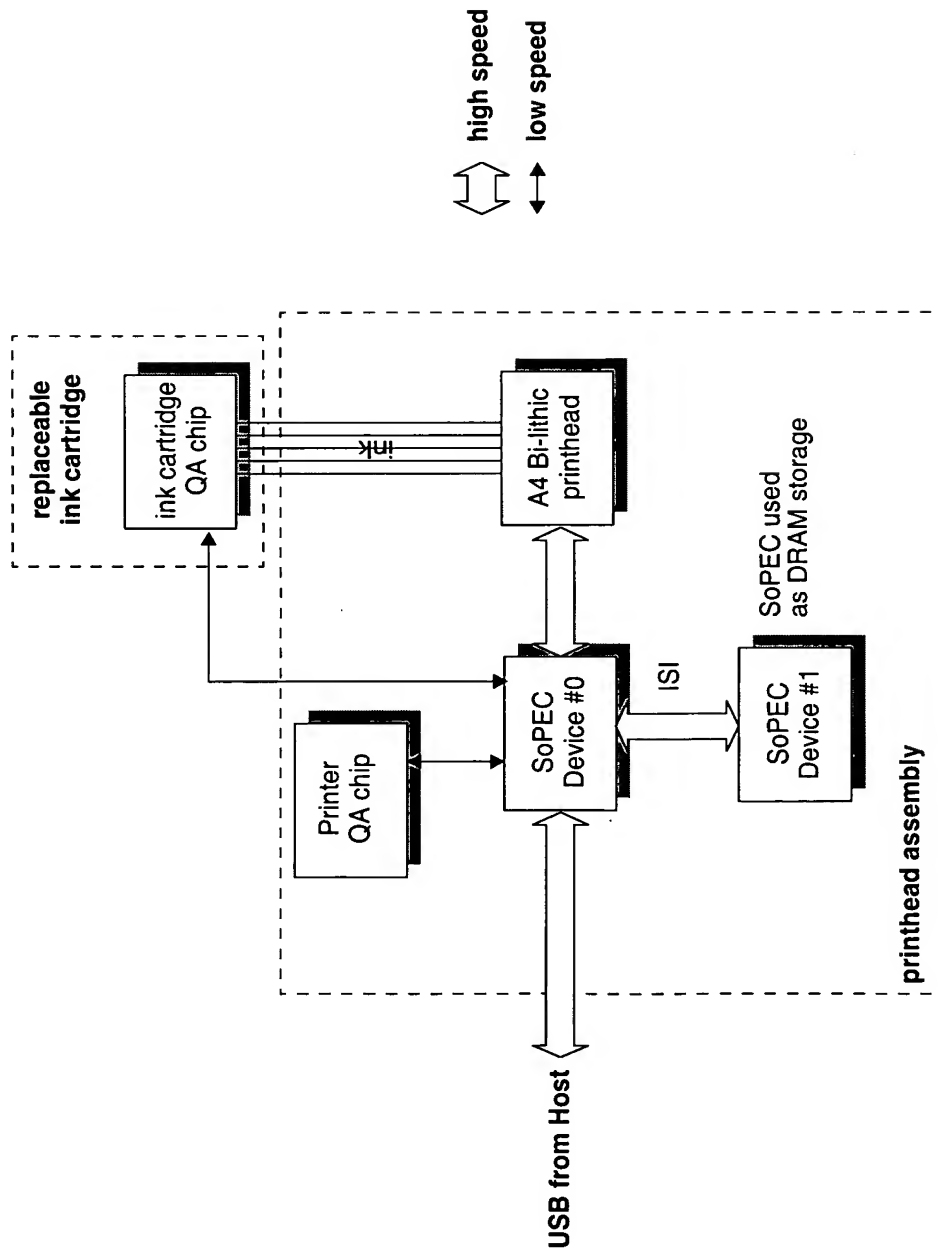


FIG. 7

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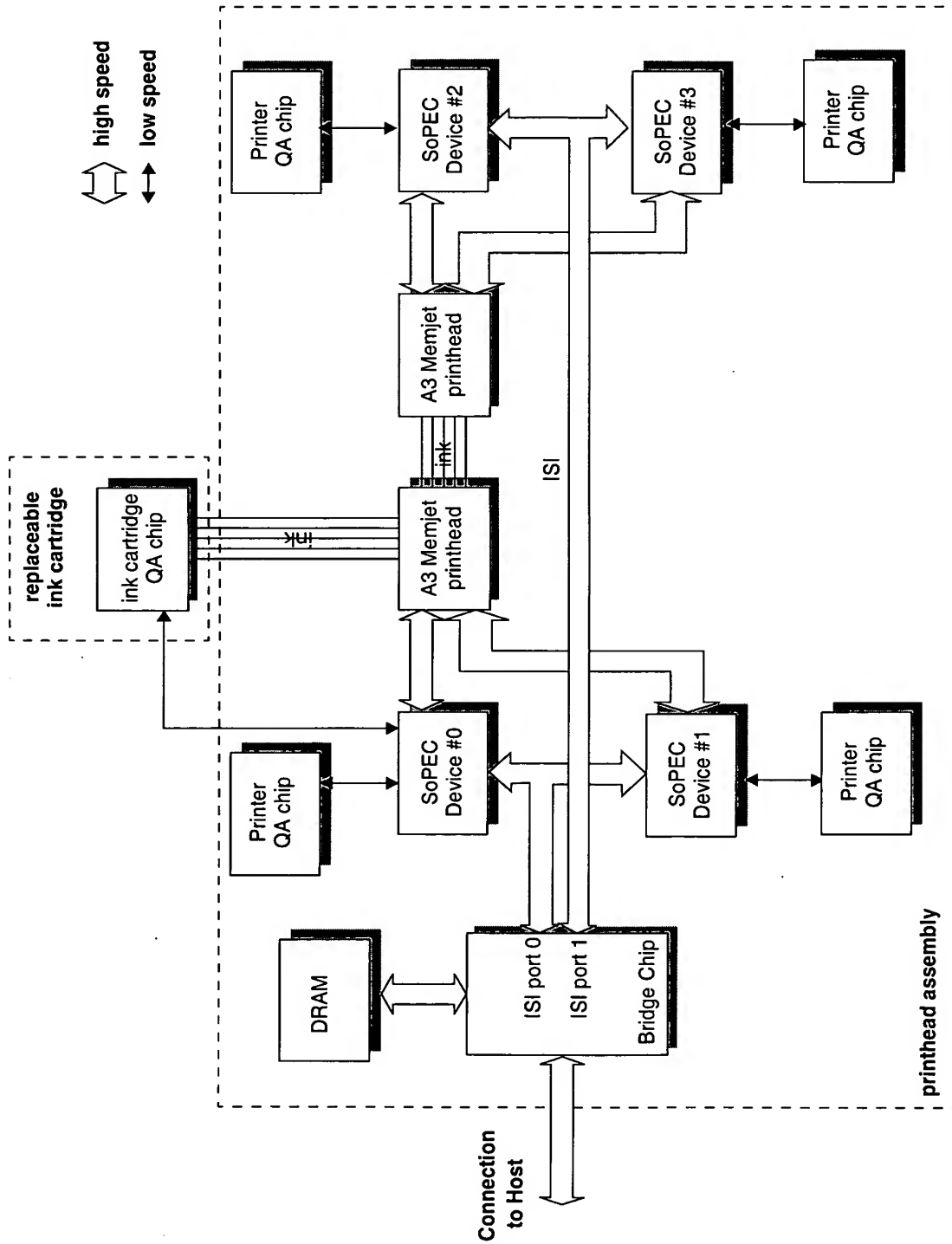


FIG. 8

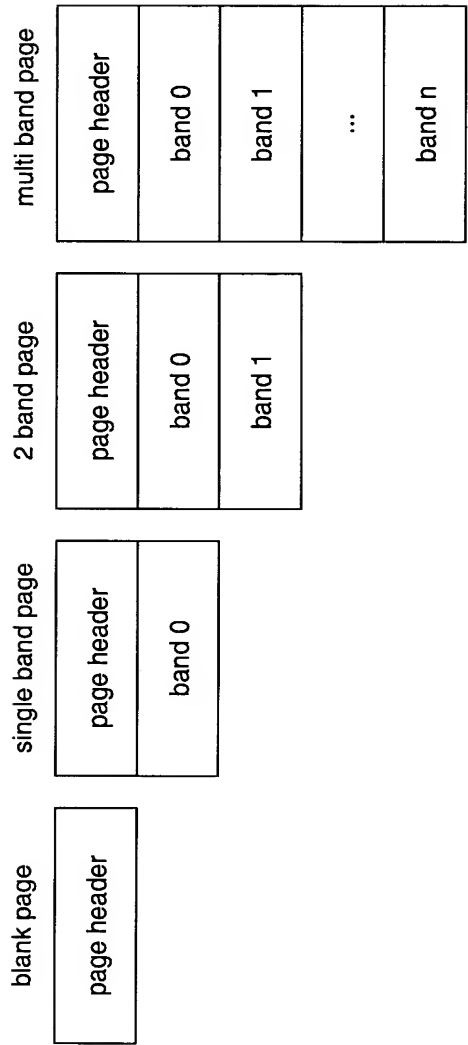


FIG. 9

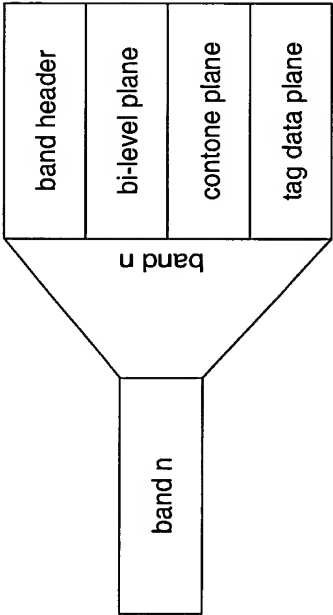


FIG. 10

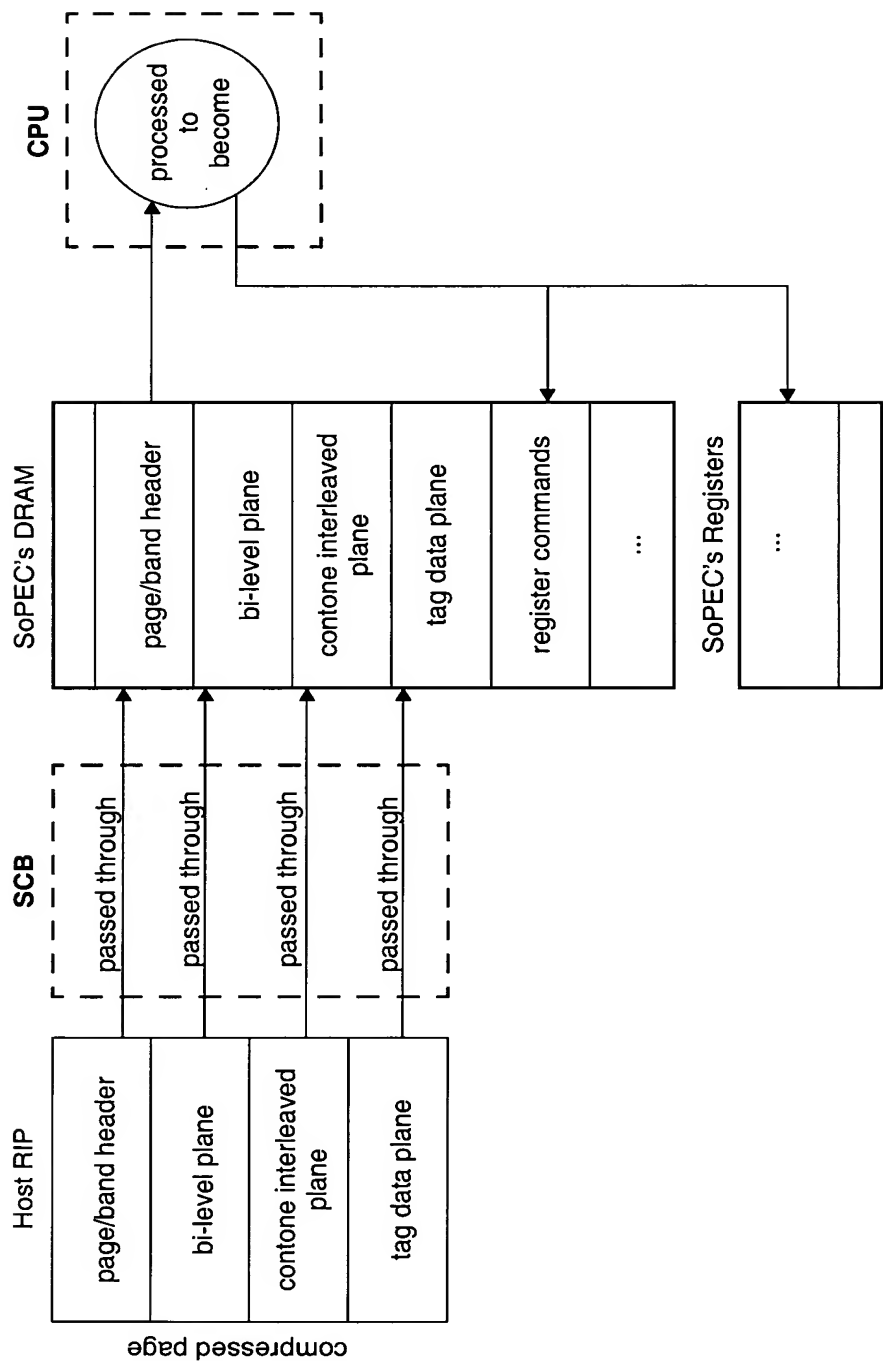


FIG. 11

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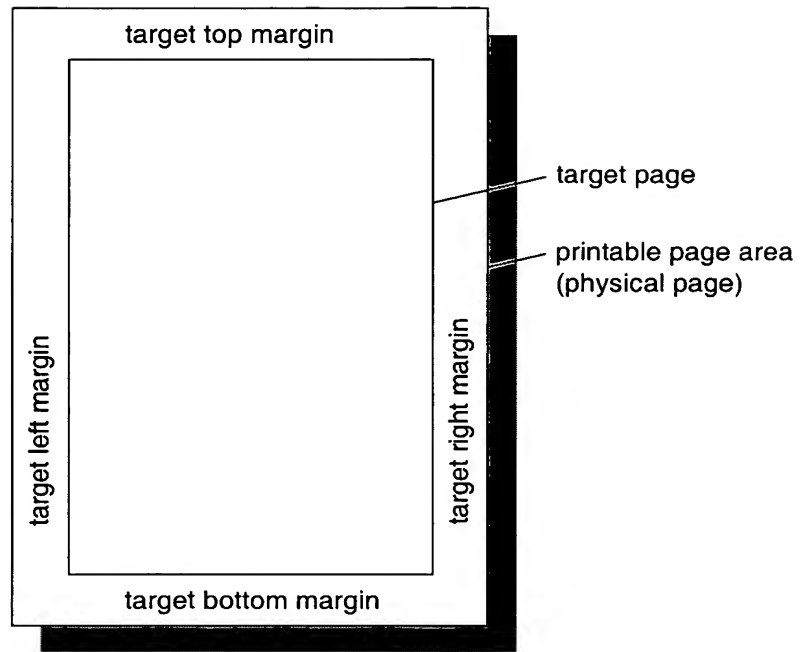


FIG. 12

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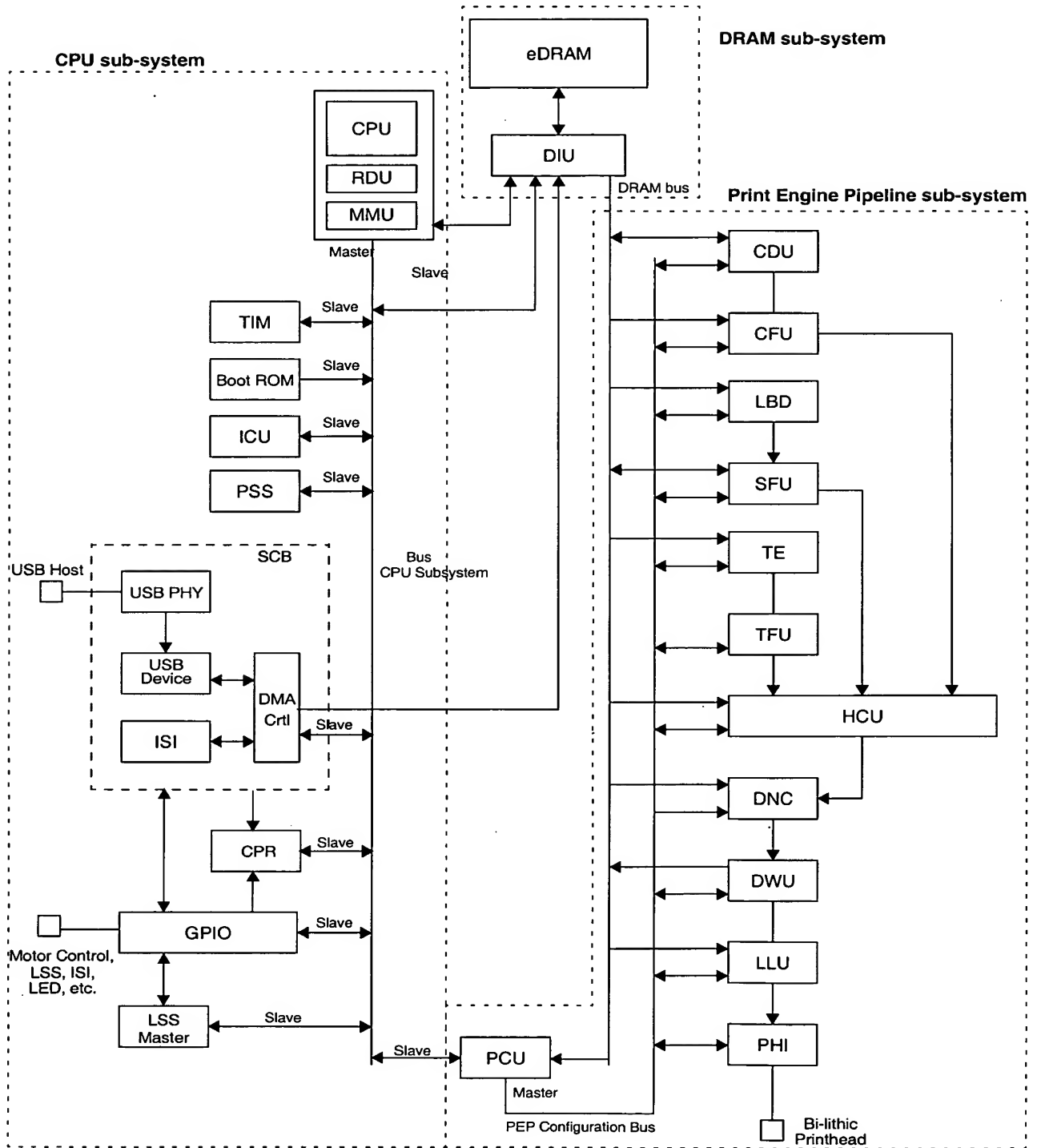


FIG. 13

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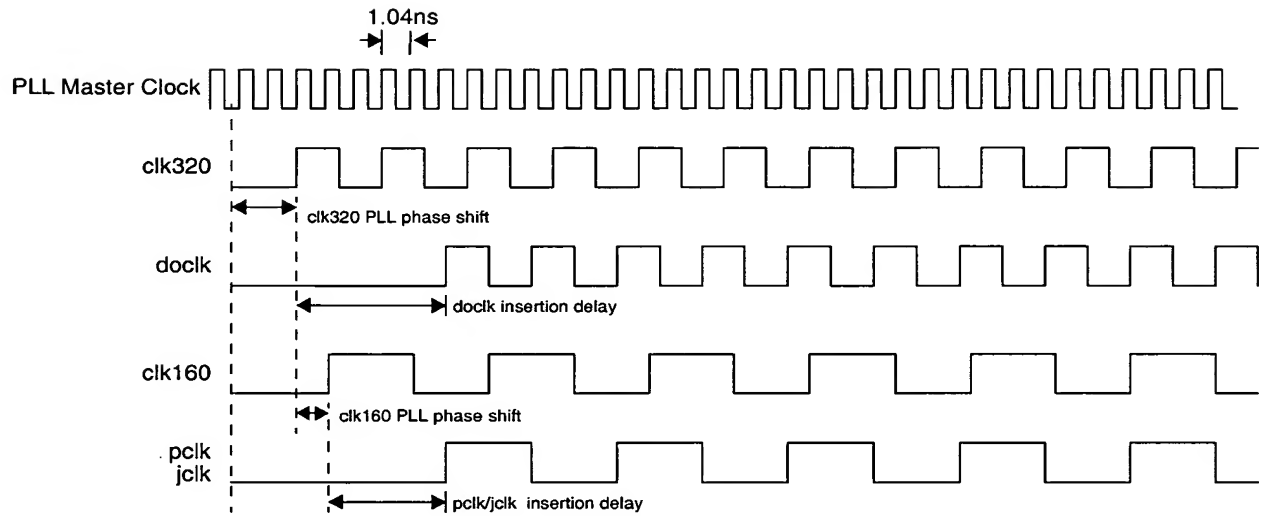


FIG. 14

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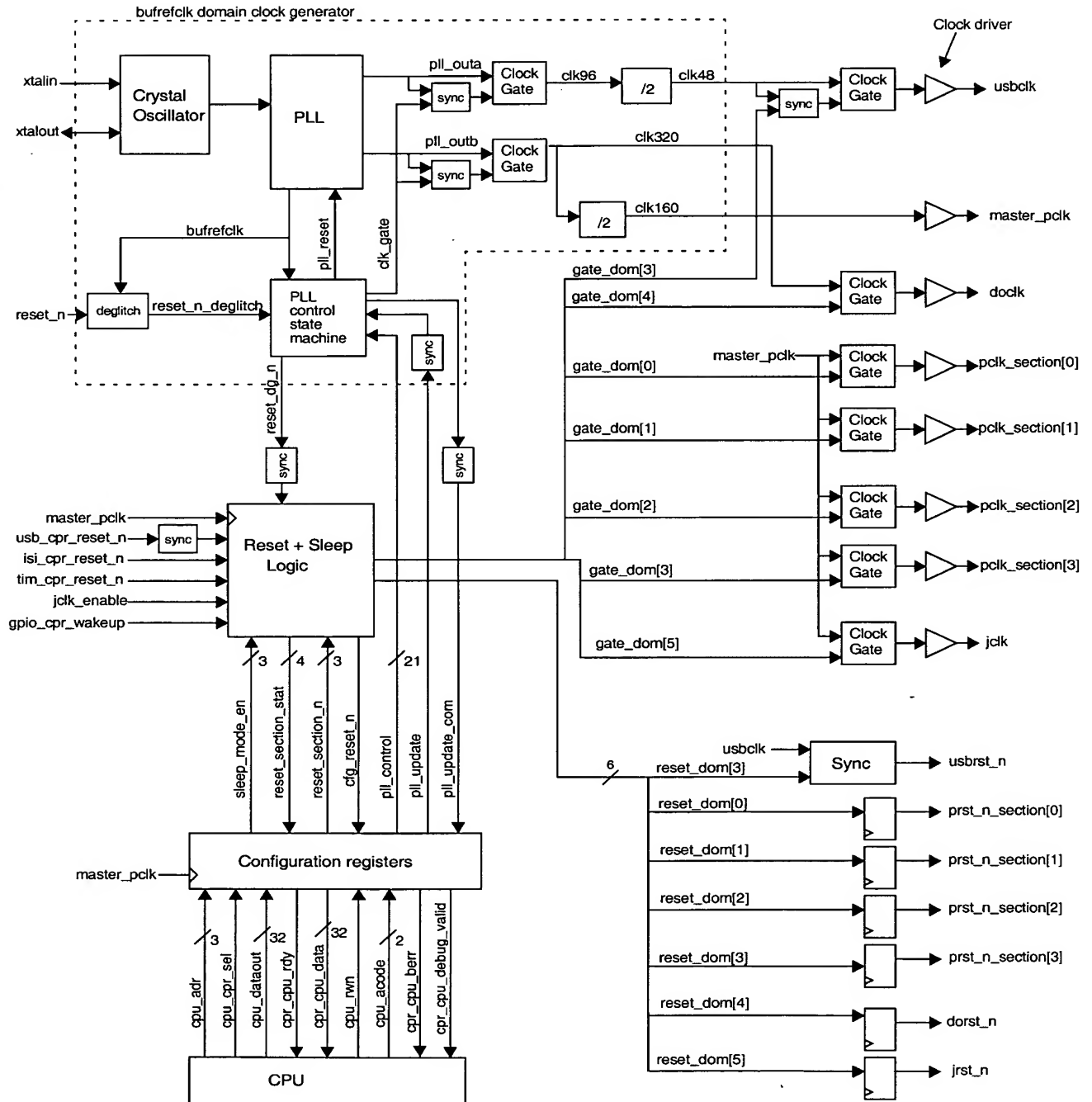
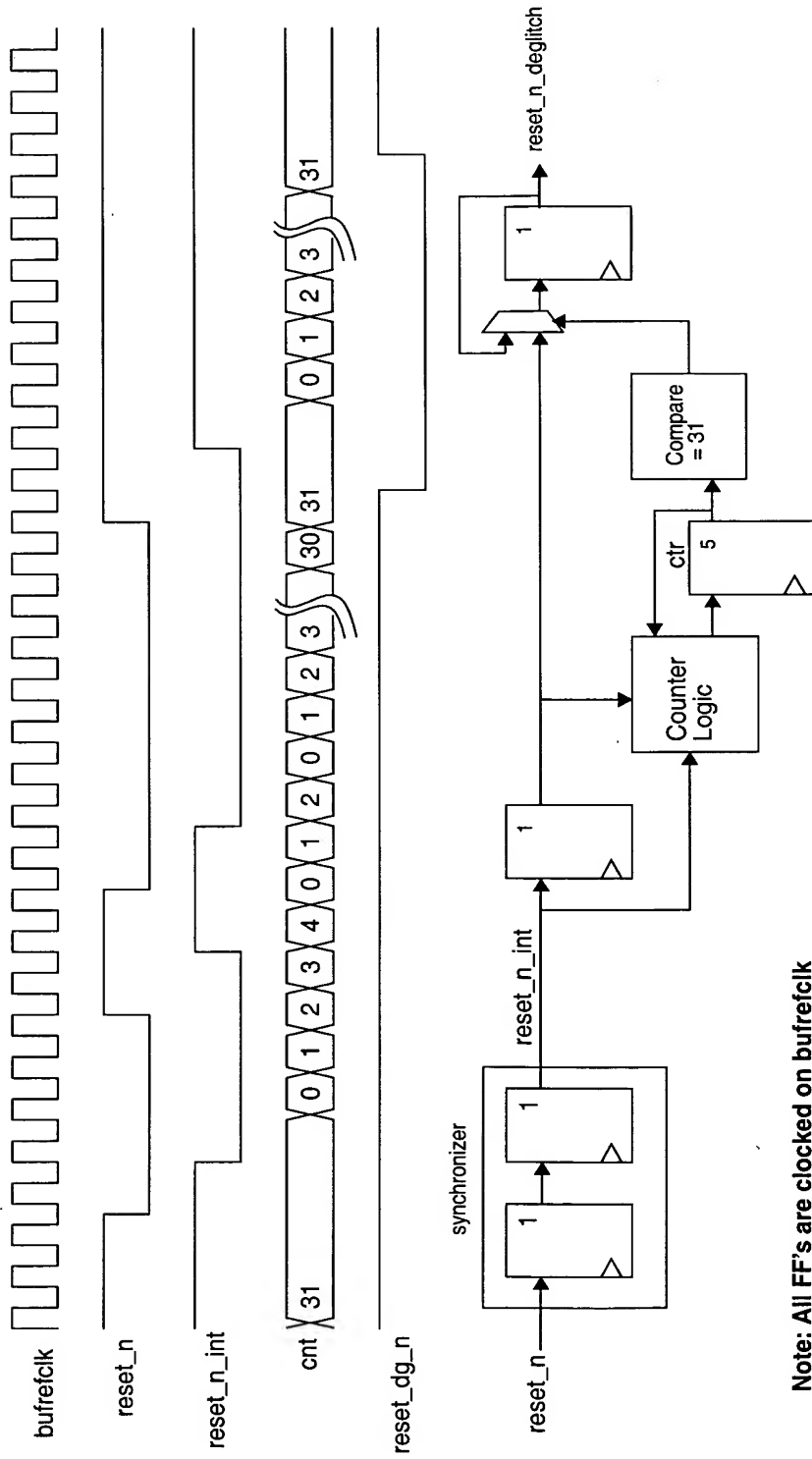


FIG. 15



Note: All FF's are clocked on bufrefclk

FIG. 16

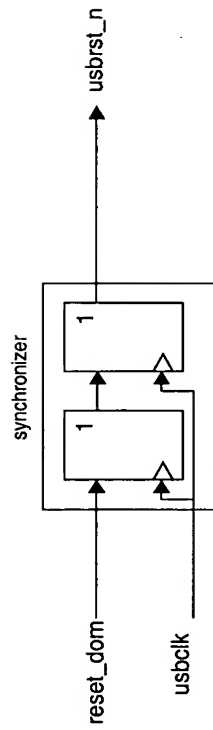
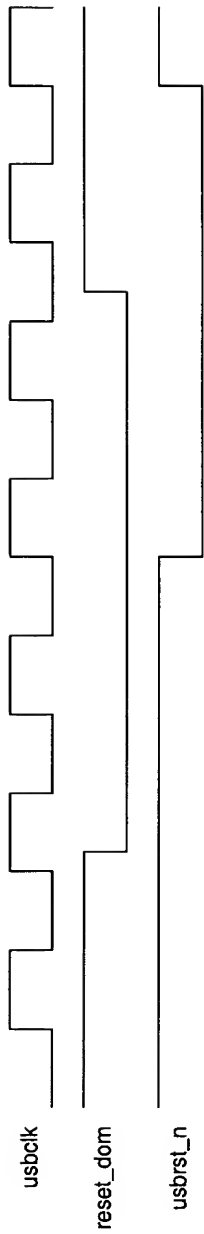


FIG. 17

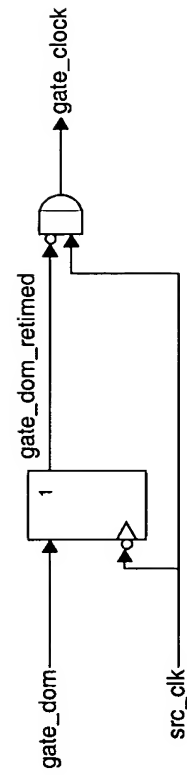
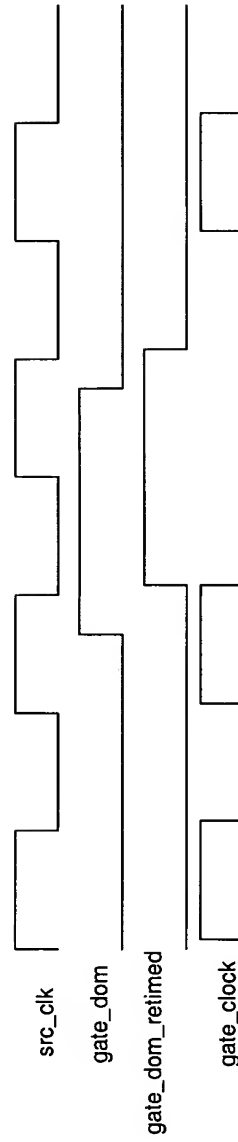
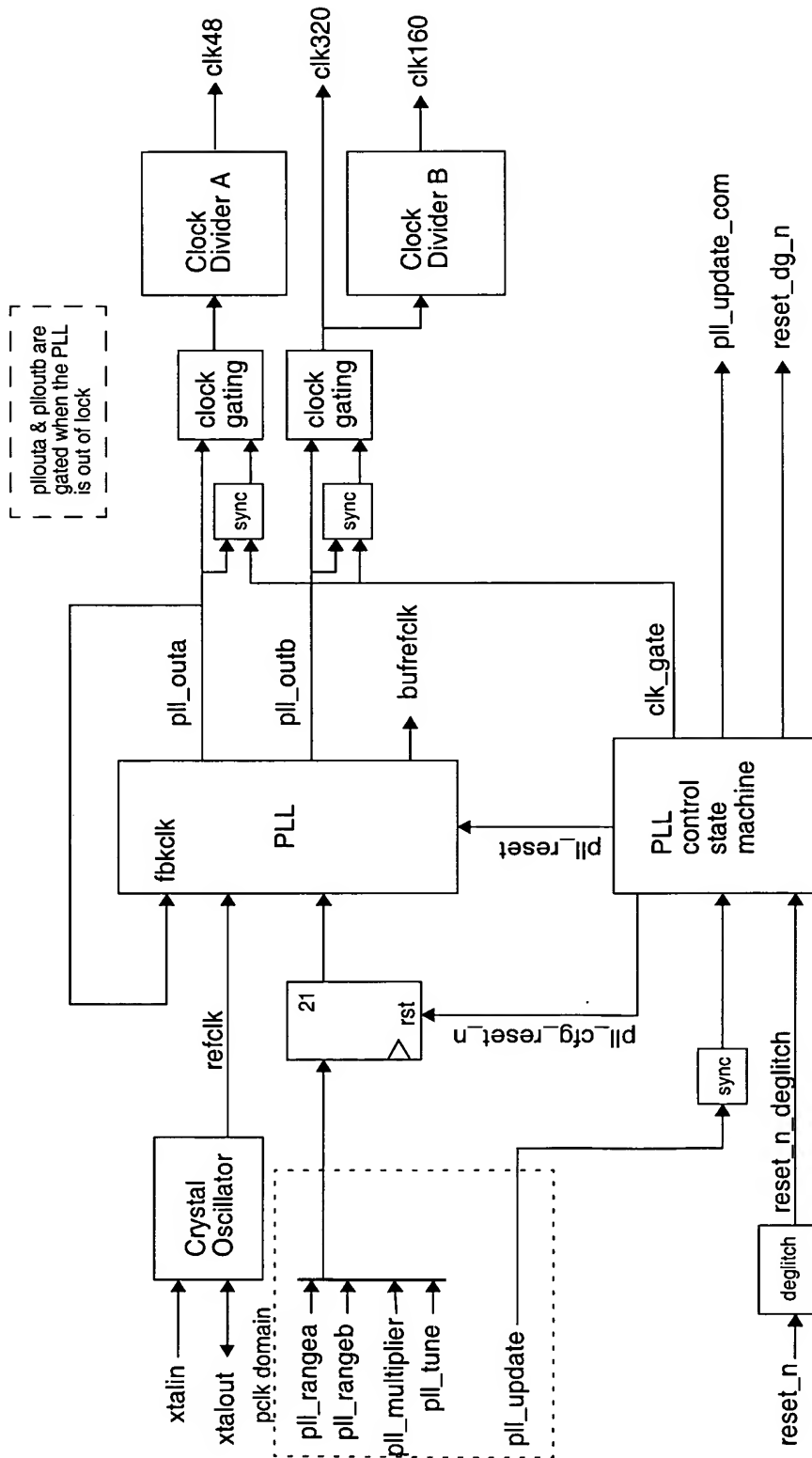


FIG. 18



Note: All logic clocked on `bufrefclk` unless otherwise indicated

FIG. 19

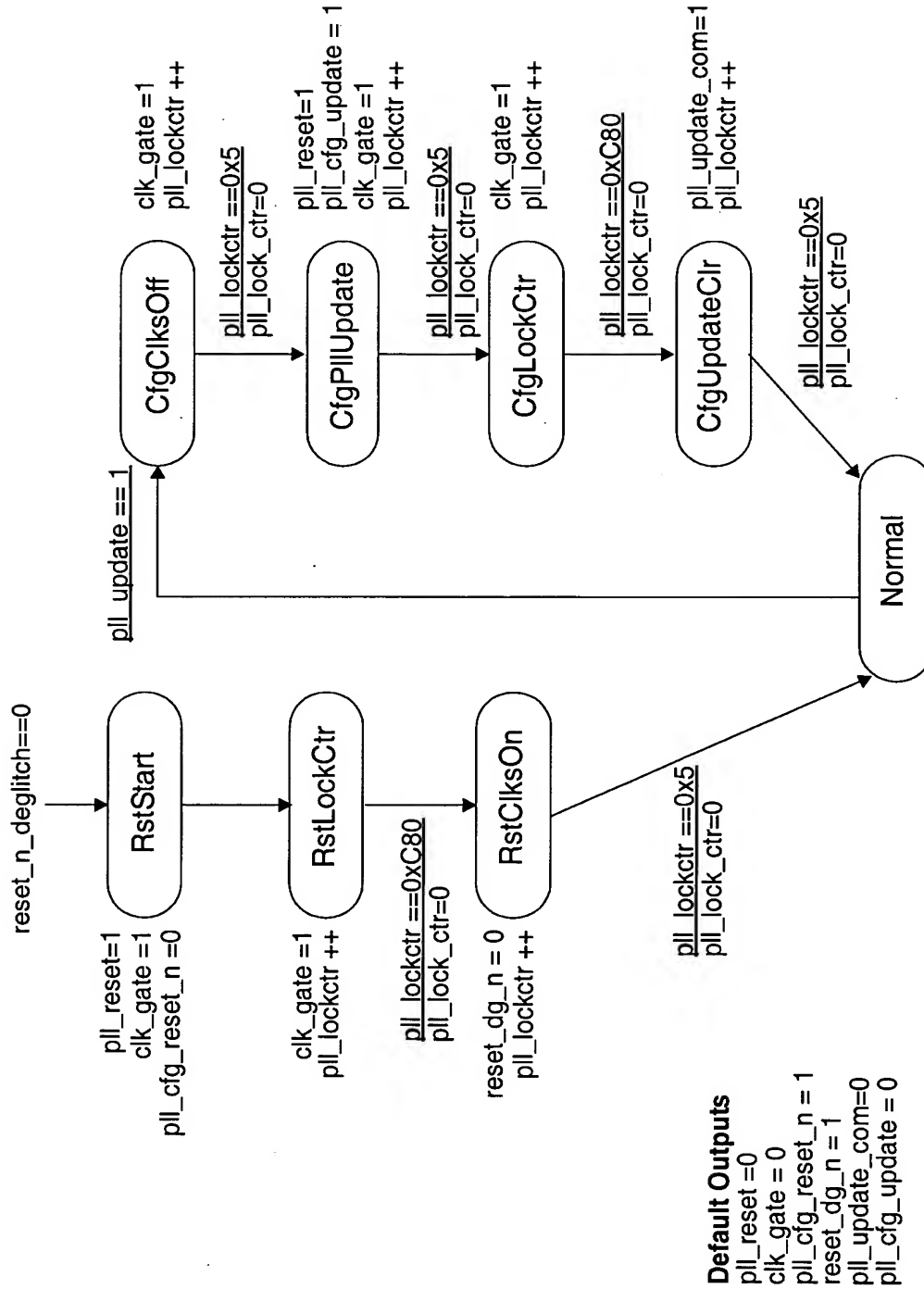


FIG. 20

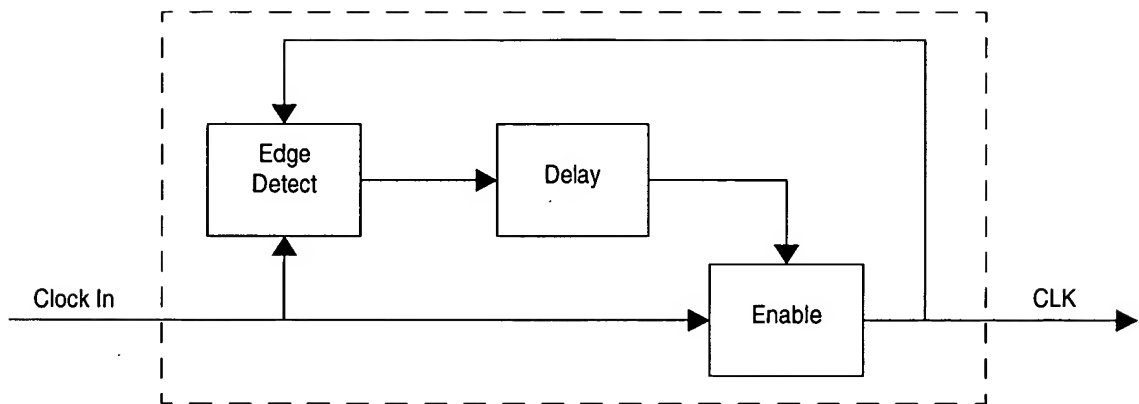


FIG. 21
(Prior Art)

Replacement Sheet

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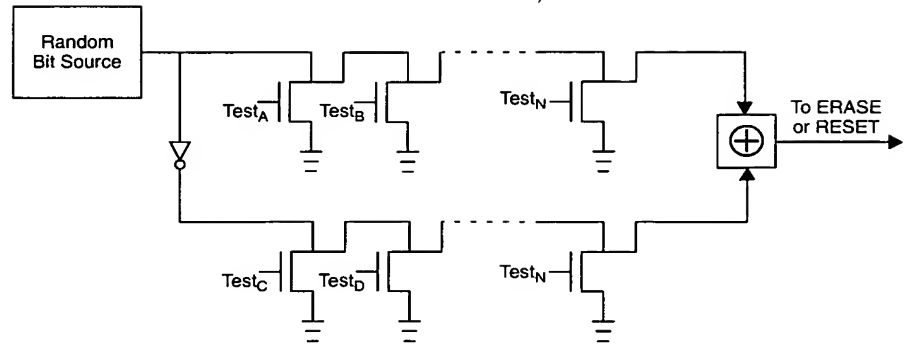


FIG. 22

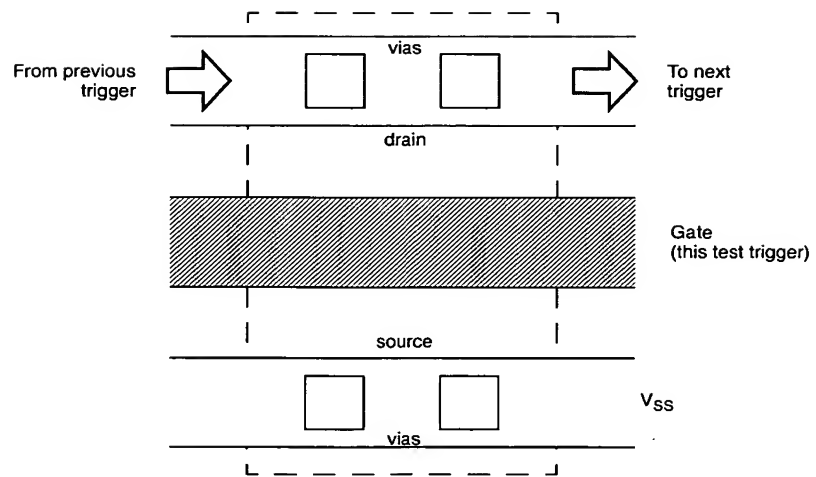


FIG. 23

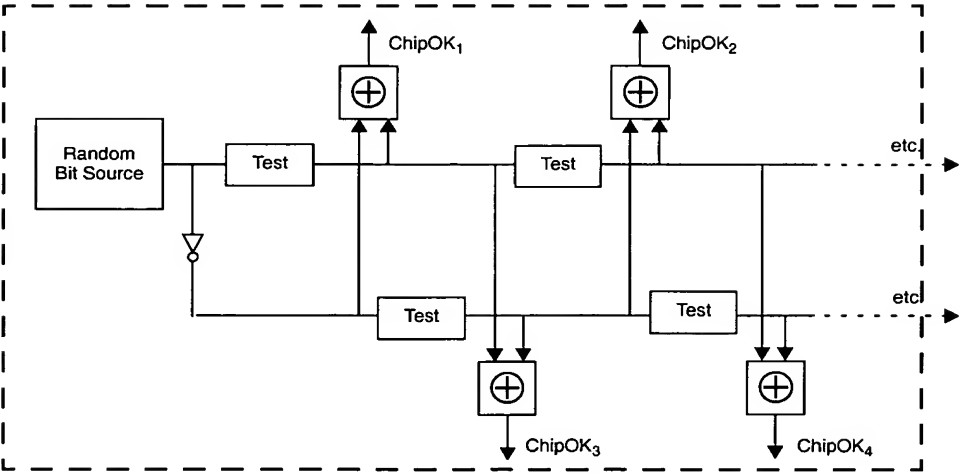


FIG. 24

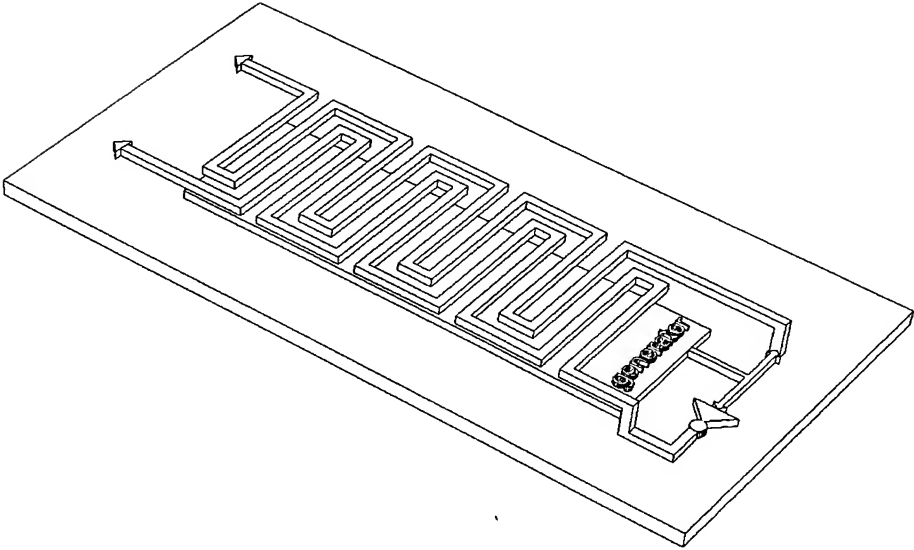


FIG. 25

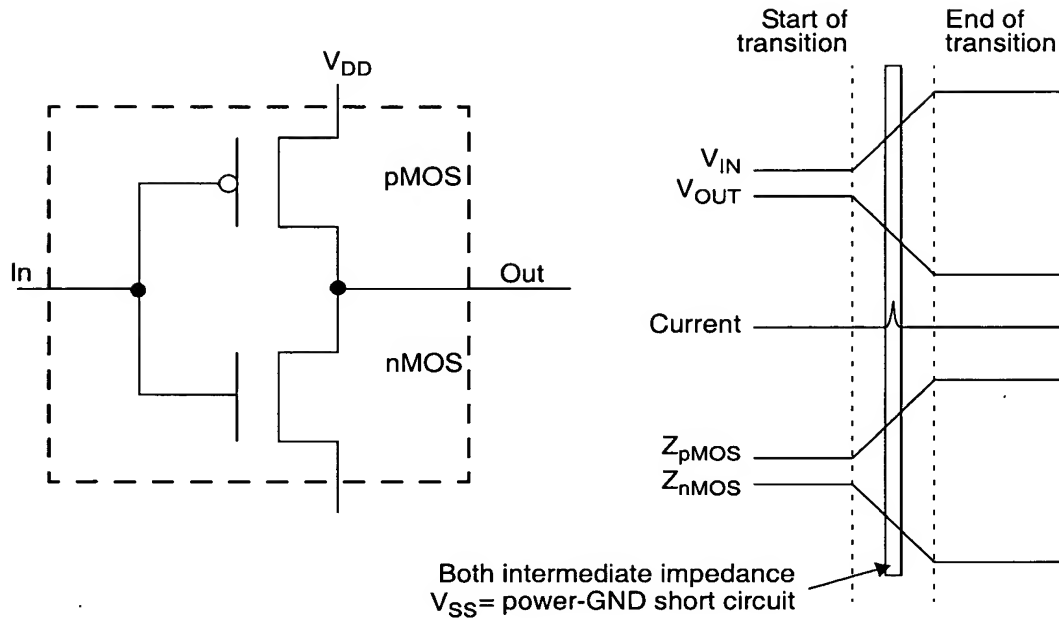


FIG. 26
(Prior Art)

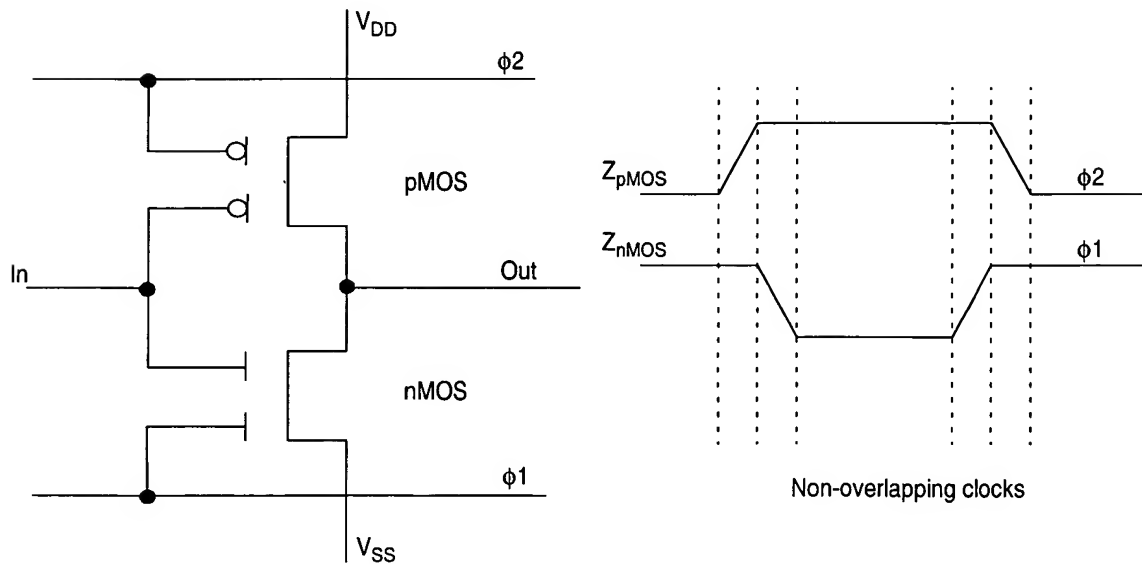


FIG. 27

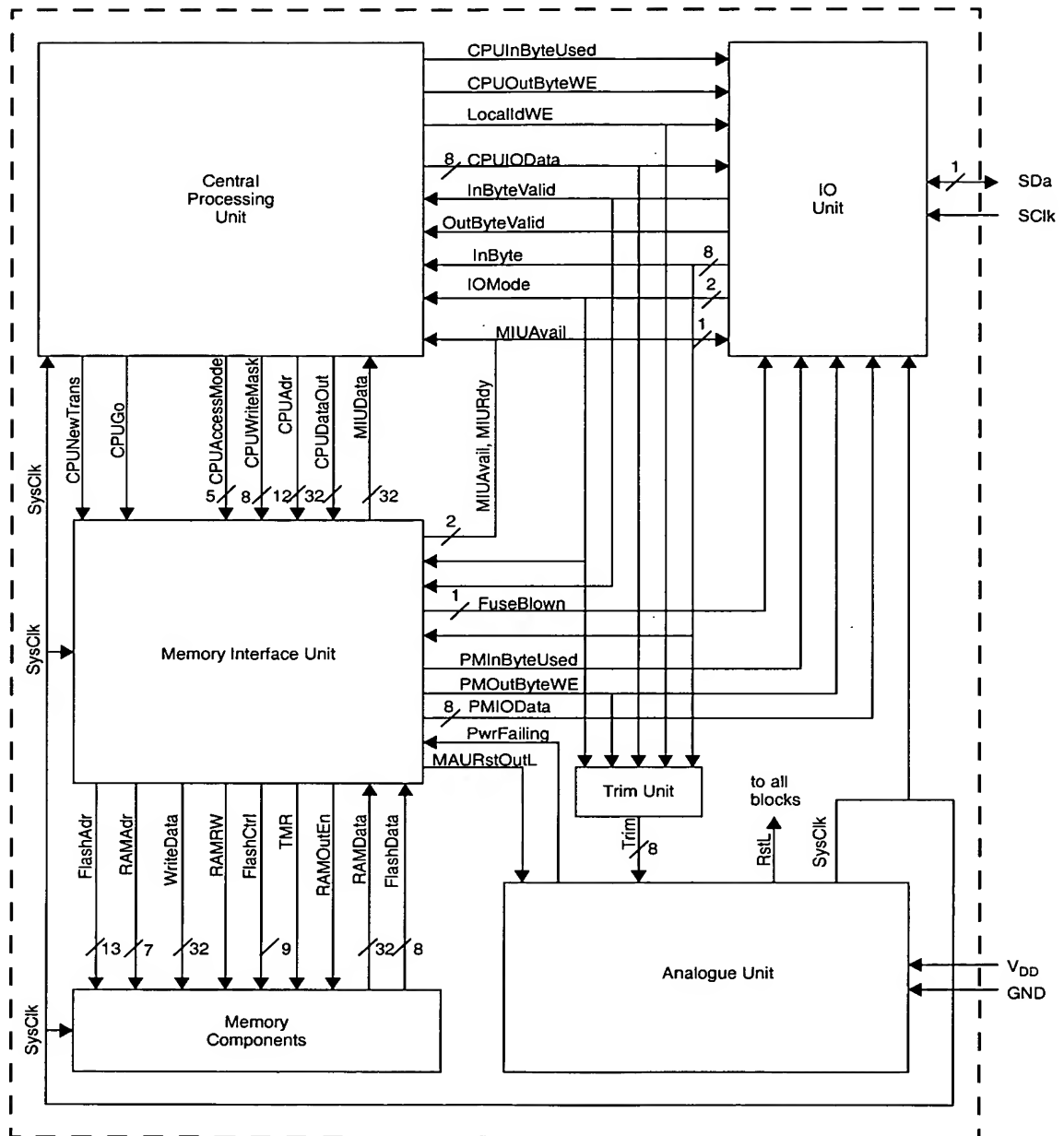


FIG. 28

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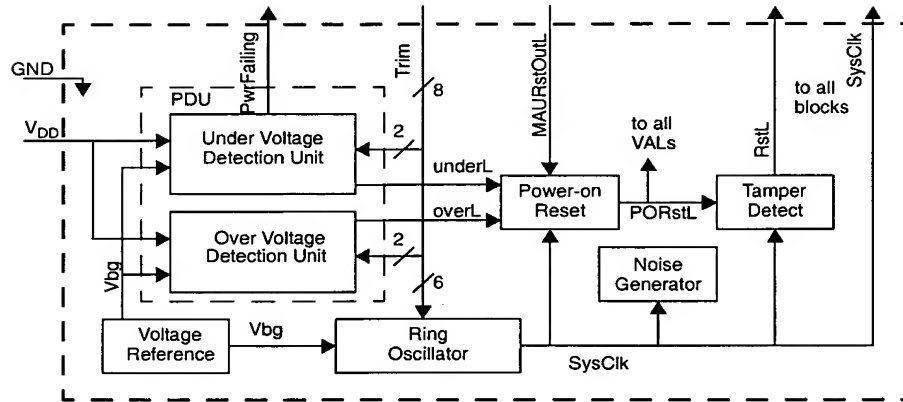


FIG. 29

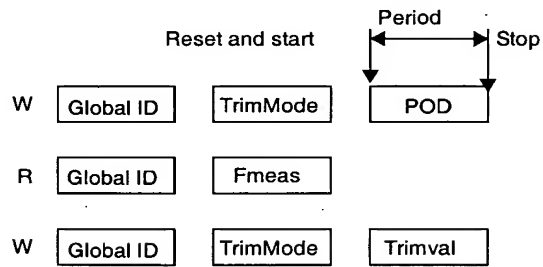


FIG. 30

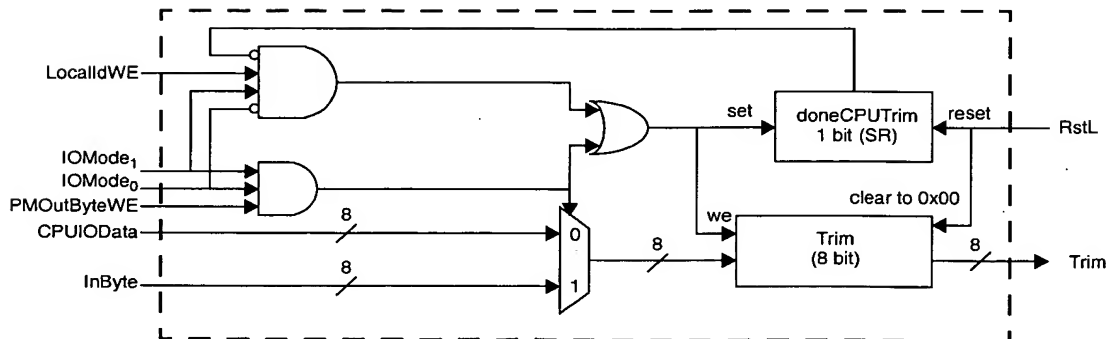


FIG. 31

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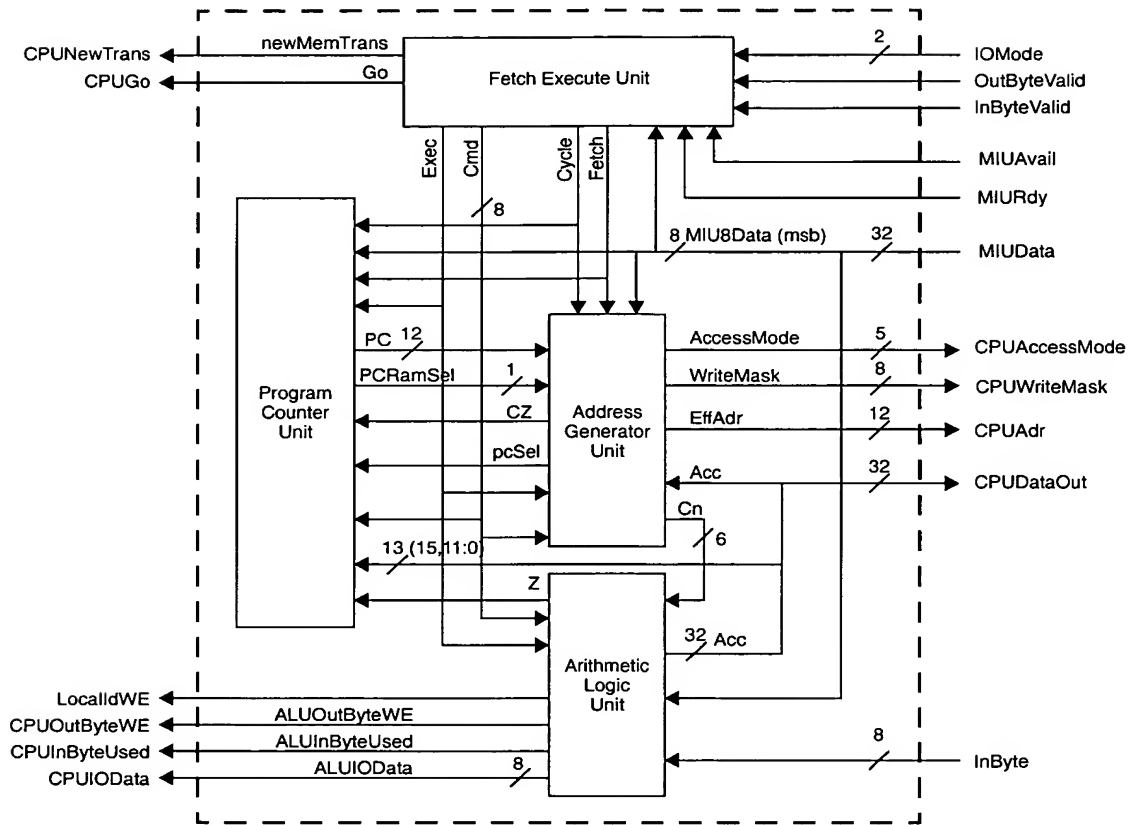


FIG. 32

Replacement Sheet

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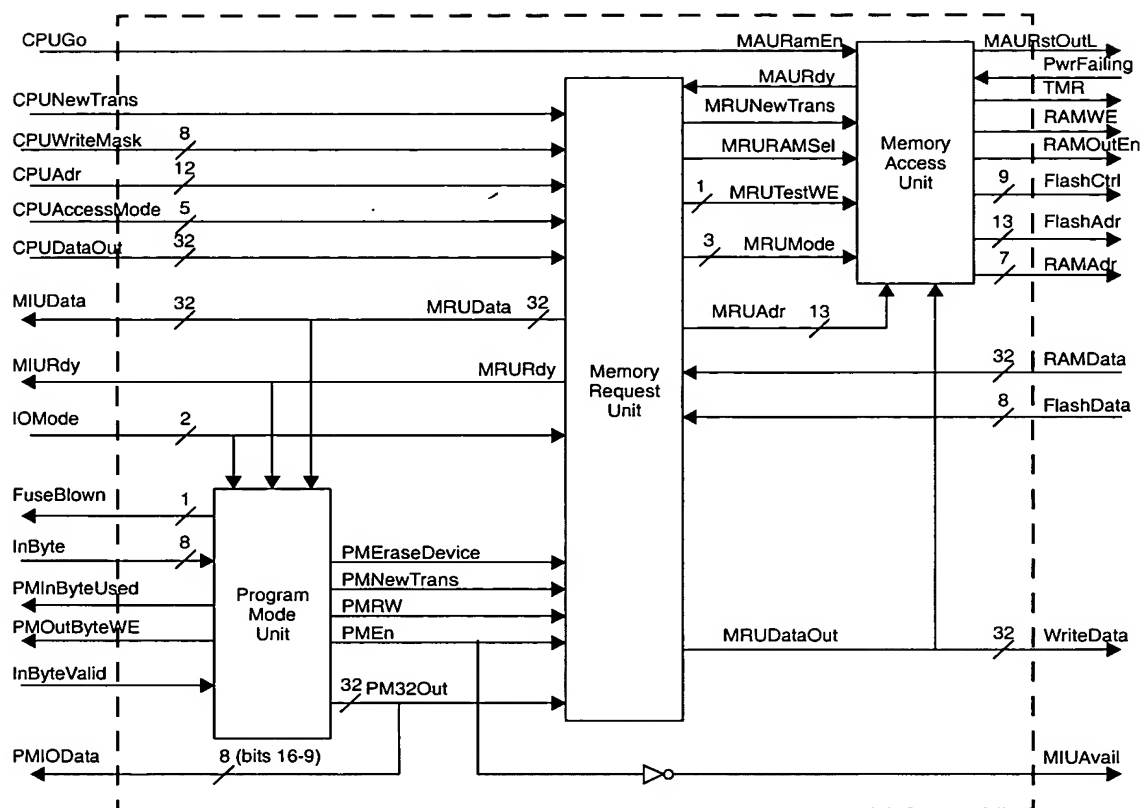


FIG. 33

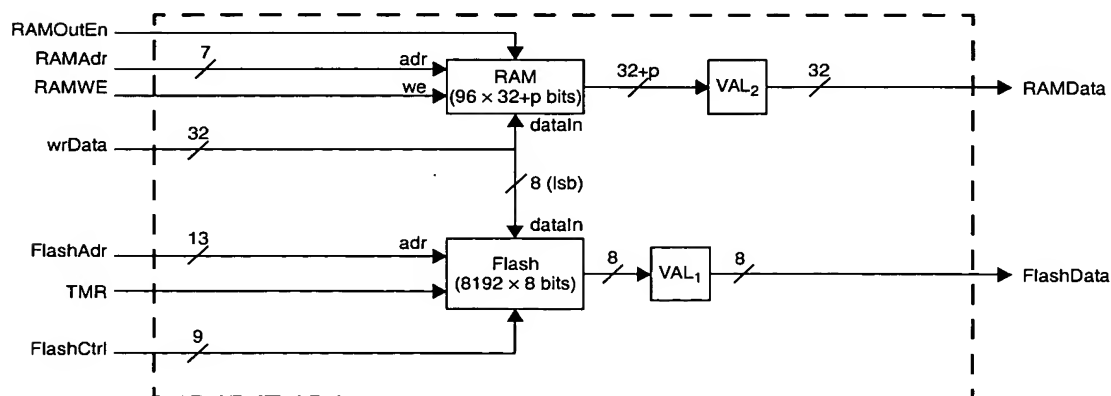


FIG. 34

Replacement Sheet

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Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PrID6	PrID5	PrID4	PrID3	PrID2	PrID1	PrID0	R/*W 0 = write 1 = read

FIG. 35

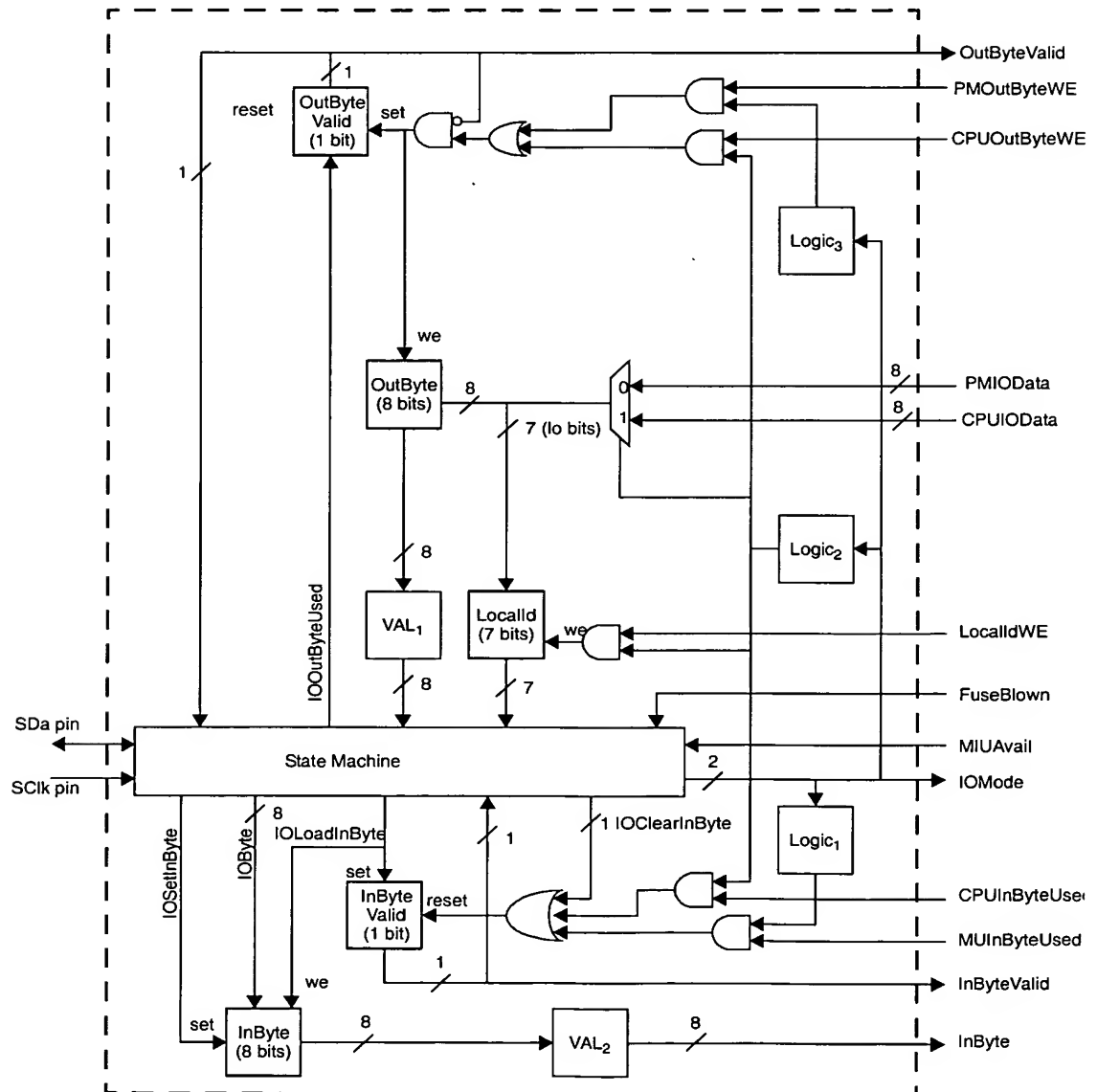


FIG. 36

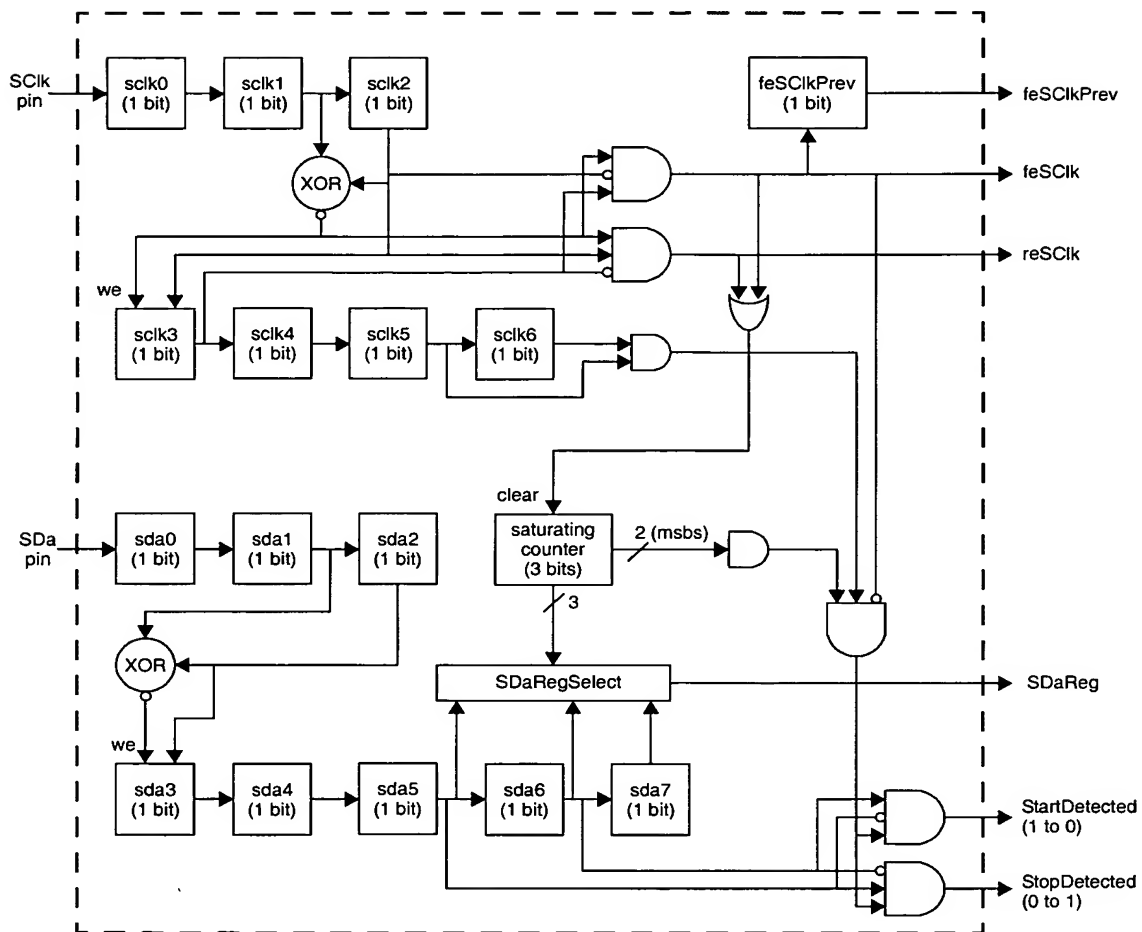


FIG. 37

Replacement Sheet

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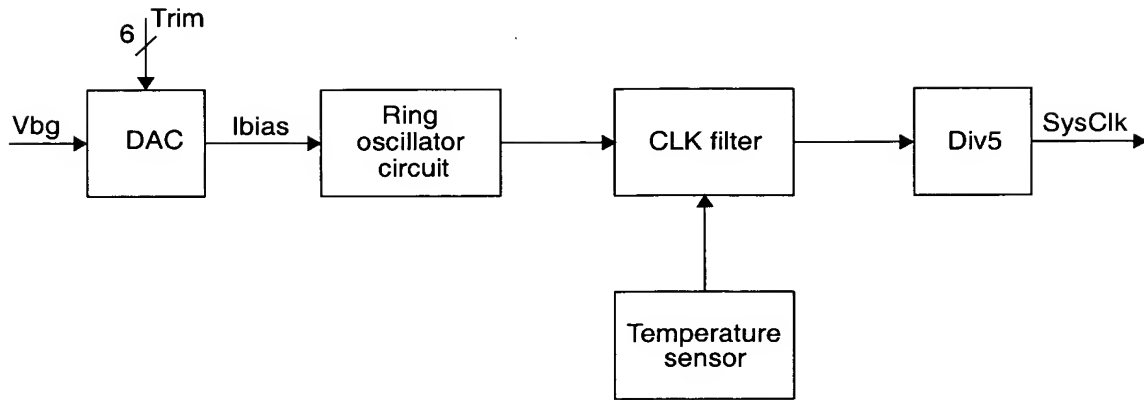


FIG. 38

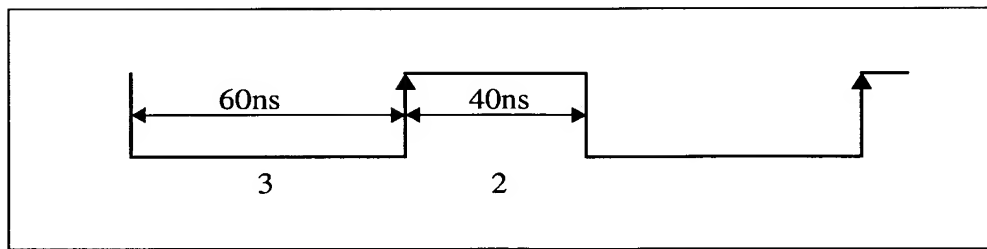


FIG. 39